

Instructor: Chris Rudell  
Email: [jcrudell@uw.edu](mailto:jcrudell@uw.edu)  
Office: M410 EEB  
URL: [http://www.ee.washington.edu/people/faculty/rudell\\_chris/](http://www.ee.washington.edu/people/faculty/rudell_chris/)  
Phone: 206-685-1600  
Office Hrs: Tue 3-4pm, Wed 2-3pm (in my office) – Or by appointment  
Special office hours on *selected* weeks in Sieg Hall: 10-11am Mon & Fri.

TA: Chenxin Su  
Email: [suc4@uw.edu](mailto:suc4@uw.edu)  
Office Hrs: TBD  
Office: TBD

Prerequisites: EE 215, EE 233, and EE 331.

Grade Distribution:	Homework and Tutorials	25%
	Projects	35 %
	Midterm 1	10 %
	Midterm 2	10 %
	Final	20 %

Simulation Tools: Cadence Spectre and MultiSim

Syllabus is subject to change depending on how the class is progressing:

- Week 1:
- Course Intro – What do electronic hardware designers build?
  - Review of CMOS device physics to include large signal operation (I/V curves).
  - Bipolar (BJT) introduction and simple device modeling.
  - *Homework 1 assigned, tutorial on VNC setup and basic operation of Cadence design tools.*
- Week 2:
- Simple Digital Inverter Design and analysis
  - *Inverter Cad Design Project assigned*
- Week 3:
- Continuation of Inverter design (for loading and fanout).
  - Return to CMOS device physics - small-signal device modeling.
  - DC biasing of CMOS devices (triode & saturation).
  - Approach to DC and small-signal (SS) circuit analysis.
  - *Homework 2 assigned*
- Week 4:
- Design and analysis of single-transistor amplifiers. Both DC and SS analysis. Begin with detailed analysis of common-source amplifier stages with and without source degeneration.

- *Common-source mini-CAD project assigned.*
  - *Homework 3 assigned.*
  - *Potential lab 1 assigned (Plotting IV characteristics of a CMOS device).*
  - *Midterm 1*
- Week 5:
- Continue with single-transistor amplifiers. Common-Gate and Common-Drain Amplifiers.
  - *Homework 4 assigned*
- Week 6:
- CMOS Source-Coupled Differential Pairs, DC transfer function, Gain and AC frequency response.
- Week 7:
- Cascode and Active Loads.
  - *Cadence and Lab assignment.*
  - *Homework 5 assigned*
- Week 8:
- CMOS Current Mirrors, and Current Sources.
  - *Midterm 2*
  - *Homework 6 assigned*
- Week 9:
- Op Amp Topologies.
  - *Final Cadence project assigned (operational amplifier design)*
  - *Homework 7 assigned*
- Week 10:
- Introduction to Stability and Two-Stage Amplifier Compensation.

**Homework:** Homework will consist of several problem sets. Late homework will not be accepted under any circumstances since the solutions will be posted immediately after the due date. To receive full credit, the homework should be stapled in order, and one-sided. The grading of the homework will emphasize the method used to arrive at the final answer, not the result itself. As a consequence, it is in your best interest to have your work arranged in a clear manner and highlight the methodology used to arrive at a solution. While you're expected to do your own homework, we encourage people to work together in groups, particularly with respect to certain simulation aspects of the assignments.

**Lectures:** Lecture attendance is not mandatory, however it is *highly* recommended as you are responsible for all material covered in class. Also, I'm quite famous for slipping random tidbits in the lecture that pop up on the midterm. Simply looking at the notes on the course website will not help, as I tend to state things verbally, without writing them down.

**Projects:**

**Tutorial:** There are tutorials for getting acquainted with the Cadence Tools. They will start with basic analog simulation, followed by the use of Spectre tools. In addition, there will be some tutorials on analog circuit simulation and layout as well.

**Course Text:** R.C. Jaeger, *Microelectronic Circuit Design*, 5<sup>th</sup> edition, New York : McGraw-Hill.